(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 800 208 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
08.10.1997 Bulletin 1997/41

(51) Int. Cl.[6]: **H01L 23/538**

(21) Application number: **97105046.3**

(22) Date of filing: **25.03.1997**

(84) Designated Contracting States:
DE FR NL

(30) Priority: **04.04.1996 JP 82262/96**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

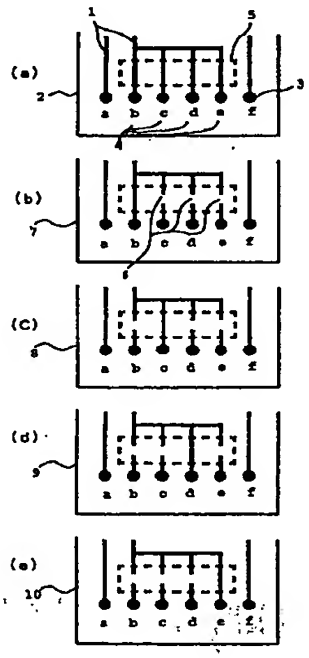
(72) Inventors:
- **Senba, Naoji**
  Minato-ku, Tokyo (JP)
- **Mikubo, Kazuyuki**
  Minato-ku, Tokyo (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) Multistage coupling semiconductor carrier, semiconductor device using the semiconductor carrier, and manufacturing method of the semiconductor device

(57) The present invention adopts a circuit pattern in which in a carrier of a package for coupling semiconductor devices at multistage, drawing out lines for selecting individual semiconductor device are coupled in parallel. Thus, the present invention achieves the multistage coupling semiconductor device which can be completed with a circuit pattern of one kind regardless of the number of stages of a multistage. Using the carrier having the foregoing structure, the semiconductor device is assembled and is subjected to characteristic inspections. Thereafter, the circuit patterns, coupled in parallel, of non-defective product of an electrical characteristic are partially cut by either laser, sand-blast, or etching. The products can be specified according to the circuit pattern which is cut.

Fig. 2



EP 0 800 208 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a carrier for a multistage coupling semiconductor, a semiconductor device using this carrier, and a manufacturing method of this semiconductor device.

2. Description of the Related Art

A semiconductor device coupled at four stages will be described as an example of a prior art. As shown in Figs. 1(a) to 1(d), in case of a first stage E board 11, the E board 11 has a pattern that among chip selector pads b to e, only pad b is connected to a multistage connection pad 23 by a pattern 21 (see Fig. 1(a)). Similar to the first stage E board 11, in case of a second stage F board 12, the board has a pattern that among chip selector pad b to e, only pad c is connected by a pattern 21 (see Fig. 1(b)). Similar to the cases of the E and F boards, a third stage G board 13 has a pattern that a connection is made only for pad d (see Fig. 1(c)), and a fourth stage H board has a pattern that only a connection is made only for pad e (see Fig. 1(d)). Specifically, in prior arts, carriers having different circuit patterns have been manufactured for the first to fourth substrates.

In the foregoing prior art, for example, in the case of the semiconductor device where four stages boards are coupled, the circuit patterns of the carriers of the boards have been different from first to fourth stages. For this reason, such semiconductor device has drawbacks that four kinds of pattern design, glass mask, carrier, and electrical characteristic inspection are necessary for four boards so that cost of the semiconductor device increases. Moreover, when non-defective percentages are different among the circuit patterns of the four boards, the yield percentage of the final product of the semiconductor device is restricted to the value of the lowest non-defective percentage. At the same time, the residual products including defective boards are treated as defective stocks. Moreover, managing cost increases because of variety of kinds of the circuit patterns.

SUMMARY OF THE INVENTION

An object of the present invention, which relates to a circuit pattern of a carrier for a multistage coupling semiconductor, is to provide a carrier for a multistage coupling semiconductor at a lower cost by reduction of the number of circuit patterns, facilitation of management and the like, a semiconductor device using this carrier, and a manufacturing method of this semiconductor device. Specifically, according to the present invention, there is provided a multistage coupling semiconductor carrier which comprises one multistage coupling pad on a board and drawing out lines for selecting more than one discrete semiconductor device; wherein the drawing out lines are coupled in parallel.

Namely, the present invention adopts a circuit pattern in which in a carrier of a package for coupling semiconductor devices at a multistage, drawing out lines for selecting individual semiconductor device are coupled in parallel. Thus, the present invention achieves a multistage coupling semiconductor device which can be completed with a circuit pattern of one kind regardless of the number of stages of a multistage.

In order to produce a semiconductor device, each multistage coupling semiconductor carrier having the drawing out lines coupled in parallel is fabricated as a semiconductor device, the drawing out line of the carrier regarded as a non-defective product of a good electrical characteristic after a characteristic inspection is partially cut to conduct multistage coupling. The cutting method is by either laser, sand-blast or etching.

Since a portion of a cut drawing out line of the carrier is not over coated with an insulating material, it can be cut precisely.

Further, since a drawing out line after partial cutting of a pattern of the carrier is coated with an insulating material such as resin, glass, alumina ceramics or the like, the cutting can be preserved.

Namely, according to the present invention, since a circuit pattern of one kind is formed regardless of the number of the multistages, management of one kind of the carrier, one kind of fabrication process and one kind of electrical characteristic inspection can be done easily, which gives the effect of much simplification of manufacturing process and improvement of yield rate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which;

Figs. 1(a) to 1(d) are plan views showing an embodiment of a prior art;
Figs. 2(a) to 2(e) are plan views of an embodiment 1 of the present invention;
Fig. 3 is a flow chart of manufacturing steps of the present invention; and
Figs. 4(a) and 4(b) are a plan view and a sectional view showing an embodiment 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described with reference to the accompanying drawings below.

(First Embodiment)

Figs. 2(a) to 2(e) are plan views showing a first embodiment of the present invention. Fig. 2(a) is an example of a circuit pattern showing a carrier in the case of four stage coupling. Multistage coupling pads 3 are formed from a to f on a common board 2. Among these pads, b to e pads are used as the chip selector pad 4. The present invention has a feature in that b to e chip selector pads are connected in parallel by the pattern 1. In addition, after completion of an electric characteristic inspection, in order to specify the first to fourth stages, the desired pattern is cut. To facilitate cutting, a pattern cutting opening 5 is formed. It is possible to increase a cutting ability by this opening.

In this embodiment, the steps up to the assembly and the electric characteristic inspection are executed using the common board 2. Thereafter, only the non-defective products are chosen to form the desired pattern thereon by laser, sand- blast, etching and the like. Thus, the first to fourth stage boards are specified. Fig. 3 is a flowchart showing manufacturing steps of the present invention.

Fig. 2(b) shows a first stage A board 7. In case of a board 7 for the first stage A, the pattern 6 connected to c to e multistage connection pads 3 is cut. Similar to the board 7 for the first stage A, in case of the board 8 for the second board B, the pattern connected to b, d and e multistage connection pads is cut (see Fig. 2(c)), and in case of the board 9 for the third stage C, the pattern connected to b, c and e connection pads is cut (see Fig. 2(d). Moreover, in case of the board 10 for the fourth stage D, the pattern connected to b to d pads is cut (see Fig. 2(e)).

(Second Embodiment)

Fig. 4(a) is a plan view showing the cutting portion of the pattern coated with an insulating material. Fig. 4(b) shows a sectional view of Fig. 4(a). The pattern 1 formed in the board 2 is cut by laser, sand-blast, etching or the like. The cut pattern 6 is coated with an insulating material 15 such as resin, glass, alumina ceramics or the like. By adopting such structure, leakage and short defects owing to migration of the pattern material as well as defects owing to external factors such as humidity, contamination or the like can be prevented. Therefore, an increase in quality can be achieved and precise cutting can be preserved.

As described above, according to the present invention, since the circuit pattern of one kind is formed regardless of the number of the multistages, costs of design, management, materials and the like concerning the pattern formation are reduced. Moreover, the present invention adopts the structure that the circuit patterns connected in parallel are partially cut as to only the non-defective products having sound electrical characteristic after the assembly and the electrical characteristic inspection, and the number of the steps is specified depending on the cut circuit pattern. Management during the manufacturing steps is made easy and the non-defective products can be effectively utilized regardless of the non-defective percentage of each stage. Thus, the stocks of the defective products in which some stages have defects are not produced as in the prior art.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

Claims

1. A multistage coupling semiconductor carrier which comprises one multistage coupling pad on a board and drawing out lines for selecting more than one discrete semiconductor device; wherein said drawing out lines are coupled in parallel.

2. A multistage coupling semiconductor carrier according to claim 1, wherein, except for at least a portion of a cut drawing out line, the carrier is over coated with an insulating material.

3. A semiconductor device comprising:

   one multistage coupling pad formed on a board; and
   drawing out lines for selecting more than one discrete semiconductor device,
   wherein a multistage coupling semiconductor carrier having said drawing out lines coupled in parallel is fabricated as a semiconductor device, said drawing out line of said carrier regarded as a non-defective product of a good electrical characteristic after a characteristic inspection is partially cut to conduct multistage coupling.

4. A semiconductor device according to claim 3, wherein a drawing out line after partial cutting of a pattern of a carrier is coated with an insulating material.

5. A manufacturing method of a semiconductor device comprising the steps of:

   fabricating a multistage coupling semiconductor carrier as a semiconductor device, said carrier having one multistage coupling pad formed on a board and drawing out lines, coupled in parallel, for selecting more than one discrete semiconductor device;
   inspecting electrical characteristics of said carrier;
   cutting partially the drawing out line of said car-

rier judged as a non-defective product of a good electrical characteristic; and

performing a multistage coupling of said carriers.

Fig. 1 (Prior Art)

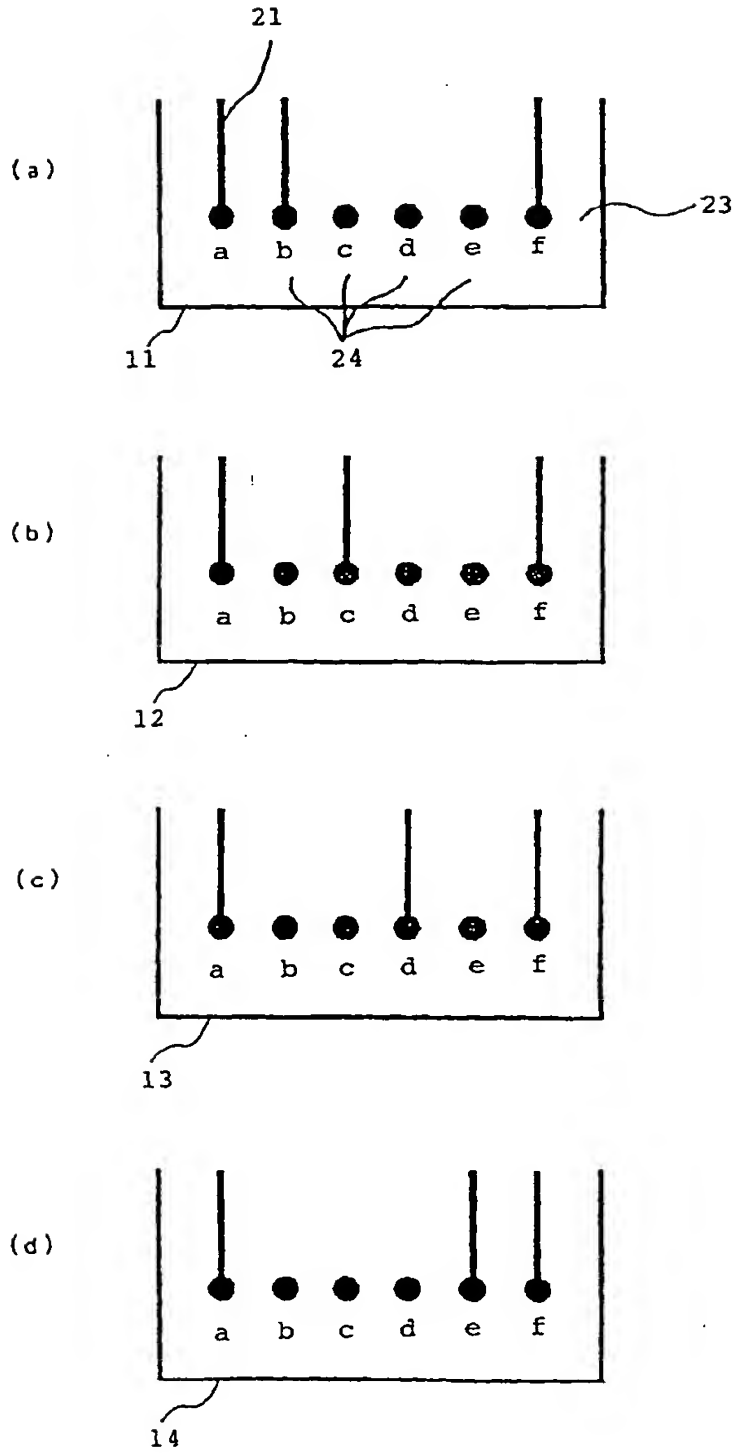


Fig. 2

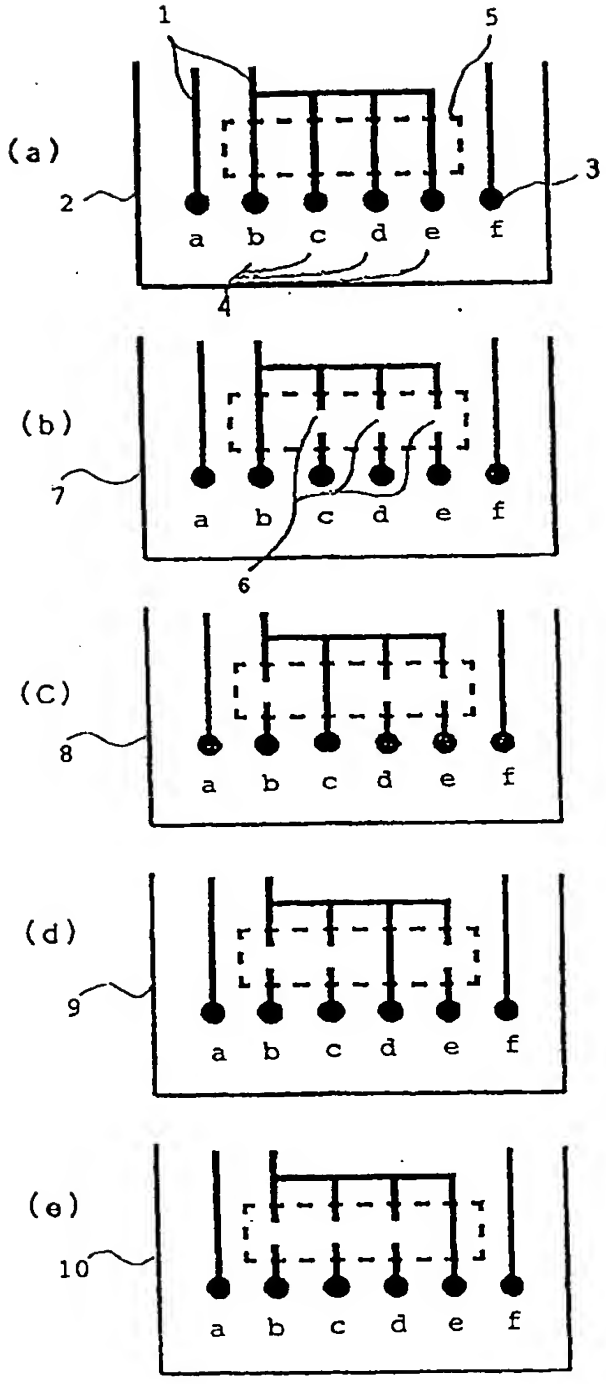


Fig. 3

FLOW OF MANUFACTURING STEPS

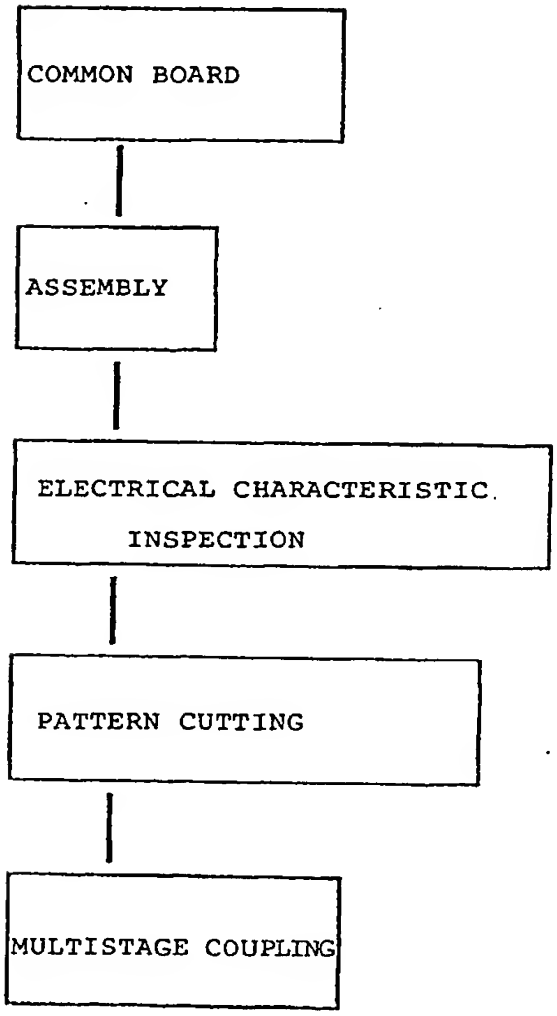
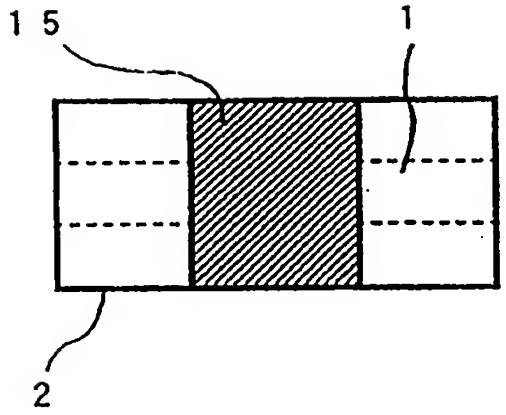


Fig. 4

(a)



(b)